**JANUMALA DEVARAJU**

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**Objective**:

TO PUT ENDLESS EFFORTS IN ACHIEVING MY GOALS AND SIMULTANEOUSLY WORKING FOR THE GROWTH OF ORGANISATION WHICH GIVES ME JOB SATISFACTION AND ALSO ENHANCE MY SKILL AND KNOWLEDGE

**Technical Skills:**

* HDL/HVL : Verilog, VHDL, System Verilog.
* Methodologies : UVM
* EDA Tools : Ncsim(Cadence)
* Operating system : Linux, Windows
* Text Editor : VIM Editor
* Version Control : SVN

**Skill Description:**

* Hands on RTL Verification using Verilog, System Verilog for 1 year
* Developing experience in building verification Environment from Scratch.
* Knowledge and working with AMBA protocols.
* Experience in building UVC’s in UVM Environment.
* Experience in developing Environments from verilog to UVM.
* Experience in writing Functional coverage’s.
* Knowledge in running Regressions for testcases.

**Training took under: “True VLSI learning centre” , Bangalore.**

**Project 1: AHB\_DAC Protocol.**

**Responsibilities :**

1. Developed the System verilog environment from scratch during training.
2. Written different test scenarios which can generate different kind of analog outputs.
3. Developed the verification plan the project.

**Language :** System Verilog

**Tools Used :** Ncsim (Cadence)

**Description :** In this project AHB is responsible for sending the digital data with higher data rates, In which the data is captured by some registers and then received by the DAC controller whose responsibility is to capture the digital data and the make it into respective analog data which represents the voltage levels which is used to control other devices.

**Project 2: APB Memory Controller.**

**Responsibilities :**

1. Written sequence for Regmodel.
2. Developed Top level Environment.
3. Implemented the verification plan the project.
4. Written test cases for different scenarios.

**Language :** UVM

**Tools Used :** Ncsim (Cadence)

**Version Control :** SVN

**Description :**  APB Memory module can use for the applications where low speed memory size of 256bits .This module will work based on APB clock frequency which can vary from 500khz-10mhz.This module can be connected to any ABP bus architecture. Mainly design contain APB slaves, memory controller , memory model and related registers . Which can be used to configure your memory controller.

**Educational Qualification:**

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| COURSE | YEAR | NAME OF THE INSTITUTE | UNIVERSITY/ BOARD | CGPA/PERCENTAGE |
| B.TECH | 2016-2019 | R.V.R. & J.C. COLLEGE OF ENGINEERING  GUNTUR,(A.P) | AUTONOMUS | 6.4 |
| DIPLOMA | 2012-  2015 | SIR C.R.R.POLYTECHNIC  ELURU  (A.P) | STATE BOARD OF TECHNICAL EDUCATION AND TRAINING | 67.21% |
| SSC | 2012 | Z.P High School, Mandadam, Guntur Dist,  (A.P) | BOARD OF SECONDARY EDUCATION | 6.2 |

**Personal Details:**

Date of Birth : 8th June -1997

Nationality : Indian

Languages known : English, Telugu

**Declaration:**

I hereby declare that all the information provided above is correct to my knowledge.

signature: JANUMALA DEVARAJU

BANGALORE.